UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

46069 7590 08/11/2008

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
PAN, DANIEL H	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/11/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,502	11/15/2003	Clair John Glossner III	YOR919990548US4 (8728-341	9966

TITLE OF INVENTION: VECTOR REGISTER FILE WITH ARBITRARY VECTOR ADDRESSING

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	11/12/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

46069 7590 08/11/2008

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,502	11/15/2003	Clair John Glossner III	YOR919990548US4 (8728-341	9966

TITLE OF INVENTION: VECTOR REGISTER FILE WITH ARBITRARY VECTOR ADDRESSING

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$300	$0	$1740	11/12/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
PAN, DANIEL H	2183	712-004000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,502	11/15/2003	Clair John Glossner III	YOR919990548US4 (8728-341	9966

46069 7590 08/11/2008

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
PAN, DANIEL H	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/11/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 39 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 39 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/713,502	GLOSSNER ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 07/31/08*.

2. ☒ The allowed claim(s) is/are *3,5,6,7,8,9-11,14,16-22,25,27-33 (claims 1,2,4,12,13,15,23,24,26,34-60 have been canceled)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 03/03/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Daniel Pan/
Primary Examiner, Art Unit 2183

Reasons for Allowance

Upon further review and consideration based on applicant most recent remarks, none of the prior art of record teaches :

a) a computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array, the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file; and the pointer array includes at least one word which is updated based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one word of the pointer array, wherein the entries of the at least one word are updated as part of a same logical operation (claim 3);

b) a computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector

register architecture comprising a vector data file comprising a plurality of storage elements for storing data elements of the data vectors; a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array, the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file, the pointer array includes at least one word which is updated based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one word of the pointer array, the increment operation includes at least one of a modulo operation and a stride operation (claim 5);

c) a computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word

address decoder coupled to the pointer array, the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file, the storage elements of the vector data file are logically organized in a matrix of rows and columns, and wherein each entry of the pointer array includes an address representing the row and column of at least one element in the vector data file (claim 9);

d) a computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array, the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file, the storage elements of the vector file data are logically organized in a matrix of rows and columns, and wherein each array of the pointer array includes an address representing the row and column of a single element in the vector data file (claim 10);

e) a computer processor having a vector register architecture for processing operations that use data vectors each comprising a plurality of data elements, the vector register architecture comprising vector data file comprising a plurality of storage elements for storing data elements of the data vectors , a pointer array electrically coupled by a bus to the vector data file, the pointer array including a plurality of entries wherein each entry identifies at least one storage element in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array, the at least one storage element for storing at least one data element of the data vectors, wherein for at least one particular word in the pointer array, the at least one storage element identified by the particular word has an arbitrary starting address in the vector data file, and for any given entry in the pointer array, the at least one storage element identified by the any given entry is independent with respect to the at least one storage element identified by other entries of the pointer array (claim 11);

f) a computer-implemented method for processing operations that use data vectors each comprising a plurality of data elements, the method comprising the steps of: providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular

entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, wherein the words are addressed by a word address decoder coupled to the pointer array, updating at least one of the words based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one entry of the pointer array, wherein the entries of the of the at least one word are updated as part of a same logical operation (claim 14);

g) a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising : providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, the updating of at least one of the words based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one entry of the pointer

array, wherein the entries of the of the at least one word are updated as part of a same logical operation (claim 25);

h) a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising: providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, and

providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for each entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words, each addressable word comprising the arbitrary starting addresses corresponding to the storage elements of an individual data vector stored in the vector data file, updating at least one of the words based on one of data read out from at least one data element in the vector data file and data generated by performing an increment operation on data read from at least one entry of the pointer array, wherein the increment operation further includes at least one of a modulo operation and a stride operation on data read from at least one entry of the pointer array (claim 27);

i) a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the

method steps comprising: providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words corresponding to individual data vectors stored in the vector data file, the storage elements of the vector data file are logically organized in a matrix of rows and columns, and wherein each entry of the pointer array stores an address representing the row and column of at least one storage element of a data vector in the vector data file, the accessing of the vector data file for the data vector, wherein the data vector is addressed according to a word address of the pointer array (claim 31);

j) a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising: providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for at least one particular entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein

the entries having arbitrary starting addresses are grouped into addressable words corresponding to individual data vectors stored in the vector data file, the storage elements of the vector file data are logically organized in a matrix of rows and columns, and wherein each entry of the pointer array stores an address representing the row and column of a single storage element in the vector data file, the accessing the vector data file for the single storage element to execute an instruction of the program of instructions, wherein the single storage element is addressed according to the address of the pointer array (claim 32);

k) a program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for processing operations that use data vectors each comprising a plurality of data elements, the method steps comprising: providing a vector data file comprising a plurality of storage elements for storing data elements of the data vectors, providing a pointer array having a plurality of entries, wherein each entry identifies at least one storage element in the vector data file for storing at least one data element of the data vectors, wherein for each entry in the pointer array, the at least one storage element identified by the particular entry has an arbitrary starting address in the vector data file, wherein the entries are grouped into addressable words, each addressable word comprising the arbitrary starting addresses corresponding to the storage elements of an individual data vector stored in the vector data file, for any given entry in the pointer array, the at least one storage element identified by the any given entry is independent with respect to the at least one storage element identified by other entries of the pointer array, performing a

read or a write operation that addresses a vector in the vector data file via an index into the pointer array specifying an entry having a plurality of addresses corresponding to different elements of a vector in the vector data file, wherein the read or write operation accesses the vector to execute an instruction of the program of instructions (claim 33).

The practical application is the vector data processing (see Summary of Invention in pages 2-7).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

/Daniel Pan/
Primary Examiner, Art Unit 2183